I claim:

Sub A2 D13

1. A system comprising:

a computer having a processing unit, a main memory, and a local bus;

a device coupled to the local bus, wherein the device occupies an I/O slot which corresponds to a first communications port on the local bus, and the device has a register set which differs from a register set for a UART;

an operating system executed by the processing unit, wherein the operating system includes a procedure for accessing a register of a UART corresponding to the first communications port; and

a communications driver executed by the processing unit, comprising:

a UART emulation which in response to execution of the procedure for accessing a register of a UART, accesses storage locations in the main memory; and

an I/O handler which transfers values between the storage locations in the main memory and the register set of the device.

2. The system of claim 1, wherein the local bus comprises an ISA bus.

3. The system of claim 1, wherein the device coupled to the local bus, further comprises:

a comparator adapted for receiving a data signal from the local bus;

a pattern generator coupled to the comparator, wherein the pattern generator generates a signal for comparison with the data signal;

a counter operably coupled to the comparator, wherein the counter resets to an initial state following the comparator indicating the data signal is not equal to the pattern signal and advances toward a final state following the comparator indicating the data signal equals the pattern signal; and

a register coupled to the counter and adapted to receive a signal from the local bus, wherein in response to the counter reaching the final state, the register latches from the local bus a value which indicates the base address of the I/O slot occupied by the device.

Sub A3> 4. A method for communication between a computer and a device having an I/O interface which differs from the I/O interface of a UART, comprising:

coupling the I/O interface of the device to a local bus in the computer;

allocating in a memory of the computer, storage locations which correspond to registers of a UART; and

transmitting values via the local bus between the I/O interface of the device and the storage locations in the memory of the computer.

5. The method of claim 4, further comprising transmitting from an application to a communications driver a data packet which is formatted for a UART, wherein the communication driver updates a value in the storage locations according to a value in the data packet.

6. The method of claim 5, wherein the communication drive performs the step of transmitting by:

converting a value in the data packet to a converted value compatible with the I/O interface of the device; and

writing the converted value to a register in the device via the local bus.

7. The method of claim 4, wherein transmitting further comprising:

reading values from a register of the device via the local bus; and

updating the storage locations according to the value read.

8. The method of claim 7, further comprising transmitting from a communications driver to an application a data packet containing a value from the storage locations.

9. The method of claim 4, further comprising:

executing on the computer an operating environment which allocates I/O slots on the local bus for UARTs; and

setting a base device address for the device to correspond to one of the I/O slots allocated by the operating environment for a UART.

Sub A4 10. The method of claim 9, wherein setting the base device address comprises:

sensing, by the device, of a data signal on the local bus;

comparing by the data signal to a signal from a pattern generator in the device;

advancing a state indicator toward a final state in response to the data signal being equal to the signal from the pattern generator;

repeating the steps of sensing, comparing, and advancing until the state indicator reaches the final state; and

setting the base address of the device to a value indicated by a signal on the local bus in response to the state indicator reaching the final state.

11. A device for connection to a local bus of a computer, comprising:

a comparator adapted for receiving a data signal from the local bus;

a pattern generator coupled to the comparator, wherein the pattern generator generates a signal for comparison with the data signal;

a counter operably coupled to the comparator, wherein the counter resets to an initial state following the comparator indicating the data signal is not equal to the pattern signal and advances toward a final state following the comparator indicating the data signal equals the pattern signal; and

a register coupled to the counter and adapted to receive a signal from the local bus, wherein in response to the counter reaching the final state, the register latches from the local bus a value which indicates the base address of the device.

12. The device of claim 11, further comprising an address decoder adapted for receiving an address signal from a local bus of a computer, wherein the address decoder selects which data signals the comparator receives from the local bus.

13. The device of claim 11, wherein the register is adapted to latch a signal from an address line of the local bus.

14. The device of claim 11, wherein the local bus comprises an ISA bus.

15. A method for setting the base address of a device coupled to a local bus of a computer, comprising:

sensing, by the device, ~~of a~~ data signal on the local bus;

comparing by the data signal to a signal from a pattern generator in the device;

advancing a state indicator toward a final state in response to the ~~data~~ signal being equal to the signal from the pattern generator;

repeating the steps of sensing, comparing, and advancing until the state indicator reaches the final state; and

setting the base address of the device to a value indicated by a signal on the local bus in response to the state indicator reaching the final state.

16. The method of claim 15, further comprising:

placing the device in a locked state before the first sensing step, wherein in the locked state, the device does not respond to any signals sensed on the local bus; and

placing the device in an unlocked state after the step of setting the base address, wherein in the unlocked state the device responds to signals on the local bus which correspond to the set base address of the device.

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